AMENDMENTS TO THE CLAIMS:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Previously Presented) The single electron transistor as claimed in claim 6, further comprising:

a tunneling film formed between the substrate and the trap sections.

2. (Previously Presented) The single electron transistor as claimed in claim 1, wherein the gate electrode extends on the at least two trap sections.

3. (Previously Presented) The single electron transistor as claimed in claim 1, wherein the tunneling film is a silicon oxide film.

4. (Original) The single electron transistor as claimed in claim 1, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

5. (Previously Presented) The single electron transistor as claimed in claim 1, wherein the at least two trap sections are a nitride or a ferro-dielectric including PZT.

6. (Previously Presented) The single electron transistor as claimed in claim 44, wherein the trap layer includes at least two trap sections separated by the interval.

7. (Previously Presented) The single electron transistor as claimed in claim 6, wherein the at least two trap sections are a nitride or a ferro-dielectric.

8. (Previously Presented) The single electron transistor as claimed in claim 6, further comprising an insulation film covering the at least two trap sections.

9. (Previously Presented) The single electron transistor as claimed in claim 8,

wherein the at least two trap sections are sections selected from the group consisting of conductive material layers including a conductive silicon layer and a conductive germanium layer.

10. (Previously Presented) The single electron transistor as claimed in claim 8, wherein insulation film is an oxide film.

11. (Previously Presented) The single electron transistor as claimed in claim 6, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

12. (Previously Presented) The single electron transistor as claimed in claim 44, wherein the gate electrode includes conductive spacers separated by the interval.

13. (Canceled).

14. (Original) The single electron transistor as claimed in claim 12, wherein the conductive spacers are silicon spacers.

15. (Original) The single electron transistor as claimed in claim 12, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

16. (Original) The single electron transistor as claimed in claim 12, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

17. (Previously Presented) The single electron transistor as claimed in claim 12, further comprising an insulation film formed between the trap layer and the substrate, wherein the trap layer and the insulation film have a same thickness.

18. (Previously Presented) The single electron transistor as claimed in claim 55, wherein a thickness of the another insulation film is greater than a thickness of the insulation film.

19. (Currently Amended) The single electron transistor as claimed in claim 6, further comprising:

an insulation film on and between the at least two trap sections.

20. (Previously Presented) The single electron transistor as claimed in claim 19, wherein the at least two trap sections are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

21. (Previously Presented) The single electron transistor as claimed in claim 19, wherein the at least two trap sections are formed of a nitride or a ferro-dielectric.

22. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 44, further comprising:

a lower gate continuously formed on the trap layer, wherein the gate electrode includes at least two upper gates formed on an insulation film to be separated from each other by the interval.

23. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 22, wherein the insulation is an oxide film.

24. (Withdrawn-Original) The single electron transistor as claimed in claim 22, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

25. (Withdrawn-Original) The single electron transistor as claimed in claim 22, wherein the trap layer is a layer selected from the group consisting of conductive material layers including conductive silicon layers and conductive germanium layers.

26. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 19, further comprising:

a lower gate continuously formed on the insulation film; and

another insulation film formed on the lower gate , wherein the gate electrode includes at least two upper gates formed on the another insulation film to be aligned with the at least two trap sections, and to be separated from each other by the interval.

27. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 26, wherein the at least two trap sections are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

28. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 26, wherein the trap sections are formed of a nitride or a ferro-dielectric.

29-43. (Canceled).

44. (Currently Amended) A single electron transistor having a memory function, comprising:

a substrate including a source region, a channel region, and a drain region;

a trap layer formed on the substrate; and

a gate electrode opposite the trap layer, wherein at least one of the gate electrode and the trap layer has an interval therein such that at least one quantum dot having the same size as the interval can be formed ~~in a same interval~~ in the channel region, and wherein a portion of the gate electrode across the interval has a flat surface.

45. (Previously Presented) The single electron transistor as claimed in claim 44, further comprising a tunneling film formed between the substrate and the trap layer.

46. (Previously Presented) The single electron transistor as claimed in claim 44, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

47. (Previously Presented) The single electron transistor as claimed in claim 44, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

48. (Previously Presented) The single electron transistor as claimed in claim 44, wherein the trap layer is selected from the group consisting of conductive material layers including a conductive silicon layer and a conductive germanium layer.

49. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 44, wherein the interval includes at least two intervals such that at least one quantum dot can be formed in a same interval for each of the at least two intervals in the channel region.

50. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 49, wherein the at least two intervals have different widths.

51. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 1, wherein the gate electrode extends on and between the trap sections.

52. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 1, wherein the tunneling film extends between the trap sections.

53. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 1, wherein the tunneling film is on and between the trap sections.

54. (Withdrawn-Previously Presented) The single electron transistor as claimed in claim 1, wherein the tunneling film completely surrounds the trap sections.

55. (Withdrawn Previously Presented) The single electron transistor as claimed in claim 17, further comprising another insulation film formed on and between the conductive spacers.